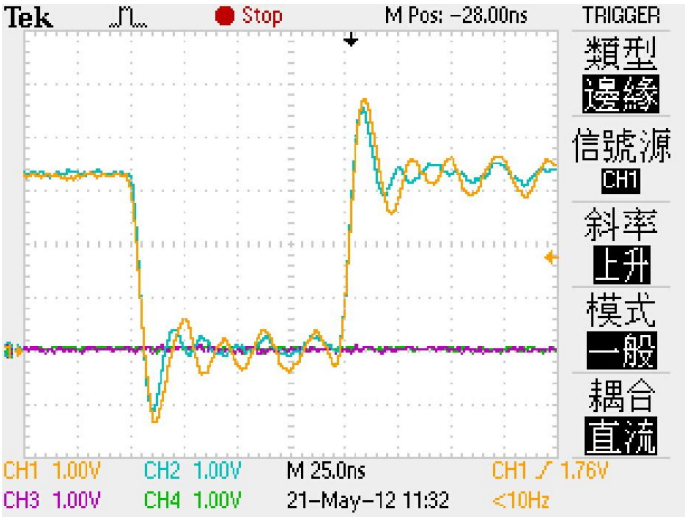
**RA8875 memory read in used STM32 FSMC**




Orange line CS; Blue line RD

As the above waveform, the FSMC read cycle of STM32F103X series shows that the rising and falling time of CS and RD is almost the same, the interval time is just about 1ns.

As the following 8080 I/F timing chart based RA8875 specification, the CS signal must be longer than RD cycle. If the CS and RD signals go up and go low at the same time, the rising signal of RD will be ignored to RA8875, and it could lead to a wrong memory read operation.

Since memory read has to execute a pre-latch manipulation, so there is one more dummy read cycle produced. If rising signal of RD is ignored, that means the pre-latch behavior for memory data read will be lost.
When we execute register read to RA8875, according to our design for RA8875, it does not need a pre-latch manipulation, that's why the register/status read do not occur a read error .

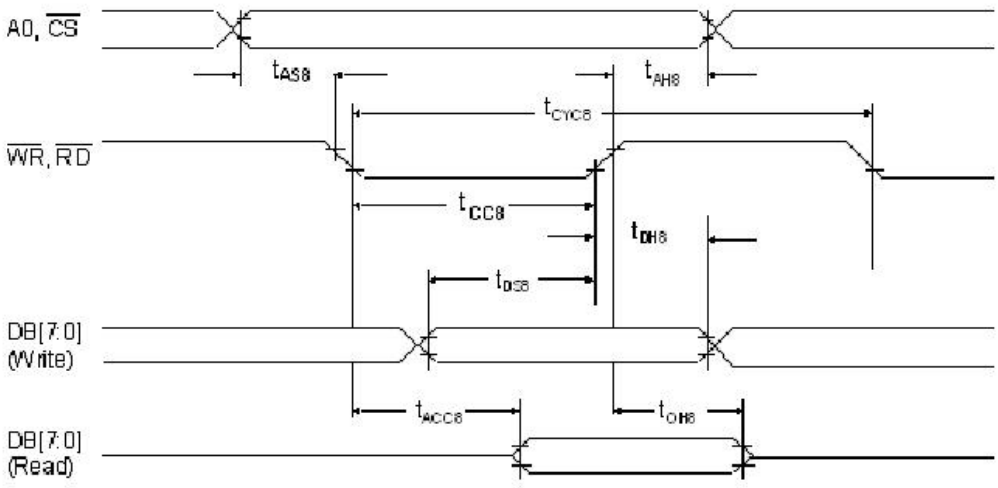



**Figure 6-4 : 8080 Waveform**

**To avoid the memory read issue, there are some solutions below:**

1. RD signal can be added pull-up resister to speed up the rising time, and CS can be added a 50pF~100pF capacitors to produce a delay for its signal.
2. Increasing the address hold time

After using STM32, we found that adjusting address hold time is ineffective. In addition, refer to the AP note of STM32 “AN2784FSMC”, we found that STM32F103x Chip FSMC timing which is used for SRAM or NORFLASH, the read cycle of CS and RD are the same, and the respective cycle time can not be adjusted. But this kind of read cycle can not work well with RA8875.